G0065

"Express Mail" mailing label number: EL846391525US
Date of Deposit: April 4, 2001
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PATENT
Docket No. P1296

TITLE OF THE INVENTION

METHOD OF FABRICATING A SEMICONDUCTOR DEVICE HAVING A NITRIDE/HIGH-K/NITRIDE GATE DIELECTRIC STACK BY ATOMIC LAYER DEPOSITION (ALD) AND A DEVICE THEREBY FORMED

CROSS-REFERENCE TO RELATED APPLICATION(S)

Not Applicable

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

Not Applicable

REFERENCE TO A MICROFICHE APPENDIX

Not Applicable

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to semiconductor devices and their methods of fabrication. More particularly, the present invention relates to the formation of gate stacks. Even more particularly, the present invention relates to forming a gate stack having superior thermal stability and reduced diffusion into silicon-bearing semiconductor structures.

2. Description of the Background Art

Currently, the semiconductor industry has an interest in reducing the critical dimensions of transistors. As such, the thickness of the gate oxide must also be reduced. In so doing, the related art has faced problems associated with a significant increase in direct tunneling leakage current through a very thin gate oxide (i.e., < 25

Angstroms). In an effort to suppress the severe gate leakage current, a high dielectric constant (high-k) material may be used as a gate dielectric, replacing a conventional thermal oxide. Several high dielectric constant (high-k) materials (metal oxides) are good candidates for gate dielectric insulators: zirconia or zirconium dioxide (ZrO_2), hafnia or hafnium dioxide (HfO_2), titania or titanium dioxide (TiO_2), tantala or tantalum pentoxide (Ta_2O_5), and the like.

However, a high-k gate dielectric insulator, such as the foregoing metal oxides, must have a thickness which is much greater than that of a conventional thermal oxide to be similarly effective, because the direct current density is exponentially proportional to a dielectric layer's thickness. Thus, the direct tunneling current flow through a gate dielectric insulator may be significantly reduced, motivating its use in for very small transistors. Another major problem with using a high-k material is thermal instability. High-k materials tend to diffuse into the silicon (Si) substrate, a polysilicon (poly-Si) gate, or a polysilicon-germanium (poly-SiGe) gate during subsequent high temperature processing steps. Therefore, a need exists for a method of fabricating a semiconductor device having a high-k dielectric gate insulator with good thermal stability which does not diffuse into the Si substrate, the poly-Si gate, or the poly-SiGe gate when experiencing subsequent high temperature processes.

BRIEF SUMMARY OF THE INVENTION

Accordingly, the present invention provides a method of fabricating a semiconductor device comprising a high-k dielectric gate insulator having good thermal stability which does not diffuse into a Si substrate, a poly-Si gate, or a poly-SiGe gate when experiencing subsequent high temperature processes, and a device thereby formed. Generally, the present invention device has a high-k gate dielectric insulator (i.e., a nitride/high-k material/nitride gate dielectric stack) formed by atomic layer deposition (ALD). The present invention method for fabricating the present device, generally comprises: depositing a first ultra-thin nitride film; depositing a high-k material film; and depositing a second ultra-thin nitride film. The unique features of the present method basically involve a sandwich structure formed by depositing an ultra-thin nitride film, which may comprise silicon nitride (Si_3N_4), before and after depositing the high-k

material film, which may comprise a thin metal film, whereby the first ultra-thin nitride film provides resistance to metal diffusion into the Si substrate, the poly-Si gate electrode, or the poly-SiGe gate electrode. This present invention device, so formed, has the advantages of providing sufficient diffusion resistance as well as thermal stability in a thin (i.e., small) feature size.

By way of example, and not of limitation, a semiconductor device having a high-k dielectric gate insulator with good thermal stability which does not diffuse into a Si substrate, a poly-Si gate, or a poly-SiGe gate when experiencing subsequent high temperature processes, may be fabricated according to the present invention by: (a) providing a substrate, wherein the substrate may comprise a silicon wafer or a silicon-on-insulator (SOI) wafer; (b) initiating formation of a nitride/high-k material/nitride gate dielectric stack by depositing a first ultra-thin nitride film on the substrate, wherein the first ultra-thin nitride film may be deposited atomic layer deposition (ALD), and wherein the first ultra-thin nitride film may comprise 1 - 2 atomic layer(s) of silicon nitride (Si_3N_4); (c) depositing a high-k material, which may comprise a thin metal film, on the first ultra-thin nitride film, wherein the thin metal film may comprise at least one metal selected from a group consisting essentially of zirconium (Zr), hafnium (Hf), titanium (Ti), and tantalum (Ta), wherein the thin metal film may also comprise a metal oxide; (d) depositing a second ultra-thin nitride film on the high-k material, thereby forming a sandwich structure, wherein the second ultra-thin nitride film may be deposited atomic layer deposition (ALD), and wherein the second ultra-thin nitride film may comprise 1 - 2 atomic layer(s) of silicon nitride (Si_3N_4); (e) completing formation of the nitride/high-k material/nitride gate dielectric stack, wherein the step (e) comprises (e)(1) depositing a thick gate material on the second ultra-thin nitride film, wherein the thick gate material may comprise a material selected from a group consisting essentially of polysilicon (poly-Si) and polysilicon-germanium (poly-SiGe); (e)(2) patterning the thick gate material, thereby forming a gate electrode; and (e)(3) etching portions of the sandwich structure uncovered by the gate electrode, thereby completing formation of the stack; and (f) completing fabrication of the semiconductor device, wherein step (f) may comprise the forming of a MOSFET structure comprising the stack, wherein the step (f) may further comprise (f)(1) forming a source/drain structure in the substrate and

flanking the stack, (f)(2) forming at least one spacer on at least one sidewall of the stack, and (f)(3) silicidizing a shallow source/drain region of the substrate as well as the stack, thereby respectively forming a source/drain silicide in the shallow region and a gate silicide on the stack.

An object of the present invention is to reduce direct tunneling current flow through a gate dielectric insulator of a semiconductor device.

Another object of the present invention is to fabricate a semiconductor device comprising a high-k dielectric gate insulator having good thermal stability which does not diffuse into a Si substrate, a poly-Si gate, or a poly-SiGe gate when experiencing subsequent high temperature processes.

Further objects and advantages of the invention will be brought out in the following portions of the specification, wherein the detailed description is for the purpose of fully disclosing preferred embodiments of the invention without placing limitations thereon.

BRIEF DESCRIPTION OF THE DRAWING(S)

For a better understanding of the present invention, reference is made to the below-referenced accompanying drawing(s) which is/are for illustrative purposes and where like reference numbers denote like elements.

FIG. 1 through FIG. 6, together, constitute a process flow diagram of the fabrication of a semiconductor device, in accordance with the present invention, wherein the semiconductor device is shown in cross-section at various stages of the process.

DETAILED DESCRIPTION OF THE INVENTION

Referring more specifically to the drawings for illustrative purposes, the present invention is embodied in the apparatus and method generally shown in FIG. 1 through FIG. 6. These figures depict an embodiment of a process for fabricating a semiconductor device comprising a high-k dielectric gate insulator having good thermal stability which does not diffuse into a Si substrate, a poly-Si gate, or a poly-SiGe gate when experiencing subsequent high temperature processes. Each figure illustrates a

particular processing stage, and presents a side view in cross-section of the device at that stage of processing. However, that the apparatus may vary as to configuration and as to details of the parts, and that the method may vary as to the specific steps and sequence, without departing from the basic concepts as disclosed herein, will be appreciated.

Referring first to Figure 1, in the first stage of processing, a substrate 10 is provided, wherein the substrate 10 may comprise a silicon wafer or a silicon-on-insulator (SOI) wafer.

Next, as shown in Figure 2, a first ultra-thin nitride film 21 is deposited on the substrate 10, thereby initiating formation of a nitride/high-k material/nitride gate dielectric stack, wherein the first ultra-thin nitride film 21 may be deposited using an atomic layer deposition (ALD) technique, wherein the first ultra-thin nitride film 21 may comprise silicon nitride (Si_3N_4), and wherein the first ultra-thin nitride film 21 may a thickness in a range of 1 - 2 atomic layer(s).

Next, as shown in Figure 3, a high-k material, such as a thin metal film 30, is deposited on the first ultra-thin nitride film 21, wherein the thin metal film 30 may comprise at least one metal selected from a group consisting essentially of zirconium (Zr), hafnium (Hf), titanium (Ti), and tantalum (Ta), wherein the thin metal film 30 also comprises a metal oxide.

Next, as shown in Figure 4, a second ultra-thin nitride film 22 is deposited on the high-k material (e.g., the thin metal film 30), thereby forming a sandwich structure 35, wherein the second ultra-thin nitride film 22 may be deposited using am atomic layer deposition (ALD) technique, and wherein the second ultra-thin nitride film 22 may comprise silicon nitride (Si_3N_4), and wherein the second ultra-thin nitride film 22 may have a thickness in a range of 1 - 2 atomic layer(s).

Next, as shown in Figure 5, a completed nitride/high-k material/nitride gate dielectric stack 40 is formed on the substrate 10, wherein the stack 40 is completed by depositing a thick gate material 31 on the second ultra-thin nitride film 22, wherein the thick gate material 31 may comprise a material selected from a group consisting essentially of polysilicon (poly-Si) and polysilicon-germanium (poly-SiGe); patterning the thick gate material 31 with a material such as a photoresist (not shown), thereby

forming a gate electrode 32; and etching portions of the sandwich structure 35 uncovered by the gate electrode 32, thereby forming the nitride/high-k material/nitride gate dielectric stack 40.

As depicted in Figure 6, a MOSFET structure 50 comprises the stack 40, wherein the MOSFET structure 50 further comprises a source/drain structure 51 formed in the substrate 10 and flanking the stack 40, at least one spacer 52 formed on at least one sidewall of the stack 40, and a shallow source/drain region 15 as well as the nitride/high-k/nitride gate dielectric stack 40 being silicidized to respectively form a source/drain silicide 16 in the shallow region 15 of the substrate 10 and a gate silicide 41 on the stack 40.

Information as herein shown and described in detail is fully capable of attaining the above-described object of the invention, the presently preferred embodiment of the invention, and is, thus, representative of the subject matter which is broadly contemplated by the present invention. The scope of the present invention fully encompasses other embodiments which may become obvious to those skilled in the art, and is to be limited, accordingly, by nothing other than the appended claims, wherein reference to an element in the singular is not intended to mean "one and only one" unless explicitly so stated, but rather "one or more." All structural and functional equivalents to the elements of the above-described preferred embodiment and additional embodiments that are known to those of ordinary skill in the art are hereby expressly incorporated by reference and are intended to be encompassed by the present claims.

Moreover, no requirement exists for a device or method to address each and every problem sought to be resolved by the present invention, for such to be encompassed by the present claims. Furthermore, no element, component, or method step in the present disclosure is intended to be dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the claims. However, it should be readily apparent to those of ordinary skill in the art that various changes and modifications in form, semiconductor material, and fabrication material detail may be made without departing from the spirit and scope of the inventions as set forth in the appended claims. No claim herein is to be construed under the provisions of 35 U.S.C. 112, sixth paragraph, unless the element is expressly recited using the phrase "means for."